

October 1987 Revised May 2002

MM74C74 Dual D-Type Flip-Flop

General Description

The MM74C74 dual D-type flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Each flip-flop has independent data, preset, clear and clock inputs and Q and \overline{Q} outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input.

Features

■ Supply voltage range: 3V to 15V

■ Tenth power TTL compatible: Drive 2 LPT²L loads

■ High noise immunity: 0.45 V_{CC} (typ.)

■ Low power: 50 nW (typ.)

■ Medium speed operation: 10 MHz (typ.) with 10V supply

Applications

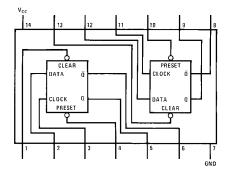
- Automotive
- Data terminals
- Instrumentation
- · Medical electronics
- · Alarm system
- · Industrial electronics
- · Remote metering
- Computers

Ordering Code:

Order Number	Package Number	Package Description				
MM74C74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow				
MM74C74N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide				

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



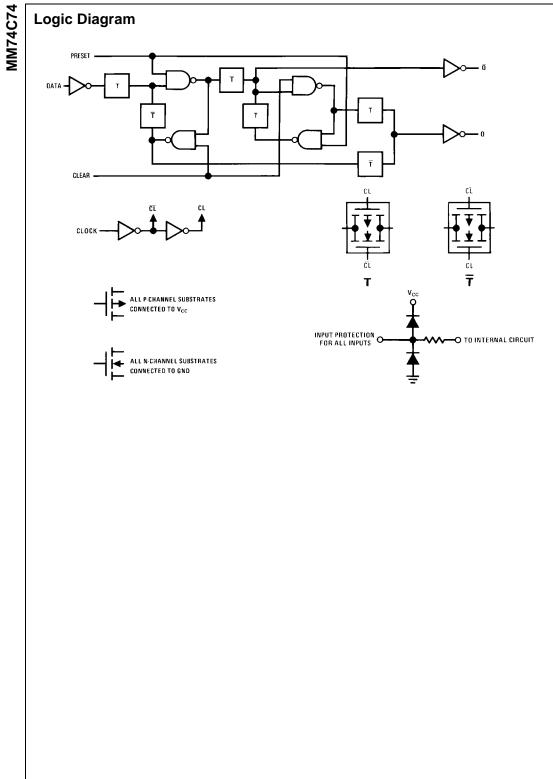
Note: A logic "0" on clear sets Q to logic "0". A logic "0" on preset sets Q to logic "1".

Top View

Truth Table

Pres	et	Clear	Q _n	\overline{Q}_n
0		0	0	0
0		1	1	0
1		0	0	1
1		1	Q _n (Note 1)	Q _n (Note 1)

Note 1: No change in output from previous state.



Absolute Maximum Ratings(Note 2)

Voltage at Any Pin (Note 2) -0.3V to V_{CC} +0.3V Operating Temperature Range -55°C to +125 $^{\circ}\text{C}$ Storage Temperature Range -65°C to +150 $^{\circ}\text{C}$

Power Dissipation

Dual-In-Line 700 mW

Small Outline 500 mW

Lead Temperature

(Soldering, 10 seconds) 260°C

Operating V_{CC} Range 3V to 15V V_{CC} (Max) 18V

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
CMOS TO	смоѕ				•	•
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 5V	3.5			V
		V _{CC} = 10V	80			
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 5V			1.5	V
		V _{CC} = 10V			2.0	· ·
V _{OUT(1)}	Logical "1" Output Voltage	V _{CC} = 5V	4.5			V
		V _{CC} = 10V	9.0			, v
V _{OUT(0)}	Logical "0" Output Voltage	V _{CC} = 5V			0.5	V
		V _{CC} = 10V			1.0	
I _{IN(1)}	Logical "1" Input Current	V _{CC} = 15V			1.0	μΑ
I _{IN(0)}	Logical "0" Input Current	V _{CC} = 15V	-1.0			μΑ
I _{CC}	Supply Current	V _{CC} = 15V		0.05	60	μΑ
CMOS/LP1	TL INTERFACE				•	
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 4.75V	V _{CC} - 1.5			
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 4.75V			0.8	V
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_D = -360 \mu A$	2.4			V
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_D = 360 \mu A$			0.4	V
OUTPUT D	RIVE (See Family Characteristics	Data Sheet)			•	
I _{SOURCE}	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$	-1.75			mA
		$T_A = 25$ °C, $V_{OUT} = 0$ V	-1.75			
I _{SOURCE}	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$	-8.0			mA
		$T_A = 25$ °C, $V_{OUT} = 0V$	-6.0			
I _{SINK}	Output Sink Current	$V_{CC} = 5V, V_{IN(1)} = 5V$	1.75			mA
		$T_A = 25$ °C, $V_{OUT} = V_{CC}$				
I _{SINK}	Output Sink Current	$V_{CC} = 10V, V_{IN(1)} = 10V$	8.0			mA
		$T_A = 25$ °C, $V_{OUT} = V_{CC}$	0.0			IIIA

AC Electrical Characteristics (Note 3)

 $T_A = 25^{\circ}C$, $C_L = 50$ pF, unless otherwise noted

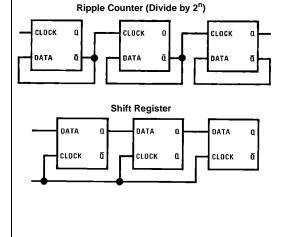
Symbol	Parameter	Conditions	Min	Тур	Max	Units	
C _{IN}	Input Capacitance	Any Input (Note 4)		5.0		pF	
t _{pd}	Propagation Delay Time to a	opagation Delay Time to a V _{CC} = 5V		180	300		
	Logical "0" tpd0 or Logical "1"	V _{CC} = 10V		70	110	ns	
	t_{pd1} from Clock to Q or \overline{Q}						
t _{pd}	Propagation Delay Time to a	V _{CC} = 5V		180	300	ns	
	Logical "0" from Preset or Clear	V _{CC} = 10V		70	110	ns	
t _{pd}	Propagation Delay Time to a	V _{CC} = 5V		250	400		
	Logical "1" from Preset or Clear	V _{CC} = 10V		100	150	150 ns	
t _{S0} , t _{S1}	Time Prior to Clock Pulse that	V _{CC} = 5V	100	50			
	Data Must be Present t _{SETUP}	V _{CC} = 10V	40	20		ns	
t _{H0} , t _{H1}	Time after Clock Pulse that	V _{CC} = 5V		-20	0	ns	
	Data Must be Held	V _{CC} = 10V		-8.0	0		
t _{PW1}	Minimum Clock Pulse	V _{CC} = 5V		100	250		
	Width $(t_{WL} = t_{WH})$	V _{CC} = 10V		40	100	ns	
t _{PW2}	Minimum Preset and	inimum Preset and V _{CC} = 5V 100		160			
	Clear Pulse Width	V _{CC} = 10V		40	70	ns	
t_r , t_f	Maximum Clock Rise	V _{CC} = 5V	15.0				
	and Fall Time	V _{CC} = 10V	5.0			μs	
f _{MAX}	Maximum Clock Frequency	V _{CC} = 5V	2.0	3.5		MHz	
		V _{CC} = 10V	5.0	8.0			
C _{PD}	Power Dissipation Capacitance	(Note 5)		40		pF	

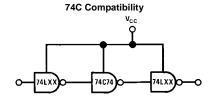
Note 3: AC Parameters are guaranteed by DC correlated testing.

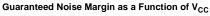
Note 4: Capacitance is guaranteed by periodic testing.

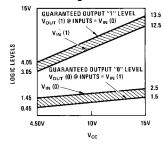
Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note—AN-90.

Typical Applications

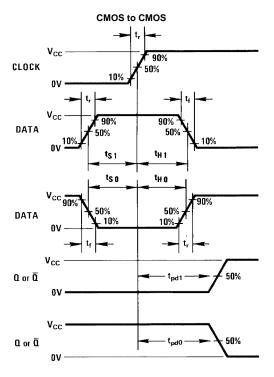






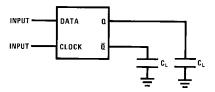


Switching Time Waveform

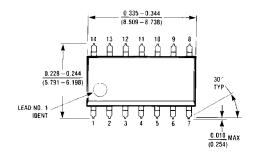


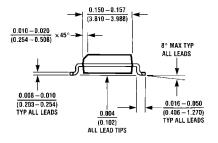
 $t_r = t_f = 20 \text{ ns}$

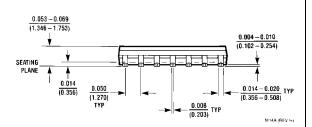
AC Test Circuit



Physical Dimensions inches (millimeters) unless otherwise noted







14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770(18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 0.250 ± 0.010 PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\overline{(7.620 - 8.128)}$ 0.065 $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 0.060 4° TYP Optional (1.524) (1.651) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 (3.175 - 3.810)0.280 (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) TYP

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

 $\frac{0.050 \pm 0.010}{(1.270 - 0.254)} \text{ TYP}$

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(0.356 - 0.584)

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0.325 ^{+0.040} -0.015 $8.255 + 1.016 \\ -0.381$

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N144 (REV.E)